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PROSKAUER ROSE LLP
ONE INTERNATIONAL PLACE
BOSTON, MA 02110

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WU, JIANYE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,053	SMITH ET AL.	
	Examiner	Art Unit	
	Jianye Wu	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/24/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments and other document filed on 4/24/2009 have been fully considered, but are moot because all independent claims have been amended. New ground rejections based on amended claims are presented in this Office Action above.

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. **Claims 3-9** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a manufacture or machine), or (2) transform underlying subject matter (such as an article or material) to a different state or thing (Reference the May 15, 2008 memorandum issued by Deputy Commissioner for Patent Examining Policy, John J. Love, titled "Clarification of 'Processes' under 35 U.S.C. 101").

Claim 3 recites "A method for transferring data comprising:

(a) packetizing …;

(b) asynchronously transmitting …; and

(c) receiving …".

The instant claim neither transforms underlying subject matter nor recites

structure associated with another statutory category, and therefore does not define a statutory process. The subject matter that does "transmitting" or "receiving" is not specified.

Claims 4-9 are also rejected because they depend from claim 3.

For examination on the merits, the claims will be interpreted as the best understood.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claim 27** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 27 recites the limitation "A computer program product, tangibly embodied in a computer-readable storage device, …", in lines 1-2, There is insufficient support in the specification for this limitation in the claim. A "computer-readable" device or medium is disclosed in Specification.

For purpose of continuation of the prosecution, the claims will be interpreted as the best understood.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

> 1. Determining the scope and contents of the prior art.
> 2. Ascertaining the differences between the prior art and the claims at issue.
> 3. Resolving the level of ordinary skill in the pertinent art.
> 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. **Claims 1-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Keenan et al (US 20030072269, hereinafter **Keenan**) in view of Luby et al., "Reliable Multicast Transport Building Block: Multirate Congestion Control", draft-ietf-rmt-bb-mrcc-00.txt, July 2000, hereinafter Luby.

For **claim 1** and **2**, Keenan discloses a method and apparatus for performing time slot switching of synchronous data across an asynchronous packet switch (44 of FIG. 2 and 3) comprising:

(a) serial to parallel interface (44 of FIG. 2 and 3) for converting time-sensitive synchronous serial data related to a plurality of source (data from telephone 38 and 39 of FIG. 3, which is time sensitive) time slots in a time-division multiplexing frame (TDM

frame 70 of FIG 5) into synchronous parallel data units (data for CBR Slot 1-4 in 70, FIG. 6 in view of 52 of FIG. 3) in accordance with a synchronous clock signal ("the system Master Clock", line 51 of Col. 28) (Notice that (a) is regarding conversion from circuit switched network to packet switched network, which is clearly disclosed either in FIG. 3 or in FIG. 4);

(b) a logic circuit (44 of FIG. 2 and 3) for formatting the synchronous parallel data units into at least first subpacket ("CBR slot 1" in frame 70 of FIG. 5) and a second subpacket ("CBR slot 2" in frame 70 of FIG. 5) in accordance with the synchronous clock signal, the first subpacket and the second subpacket being generated during a first synchronization interval of the synchronous clock signal (each subacket is transmitted in the given time slot as shown in FIG. 5); the first subpacket being associated with a first source time slot in the time-drivision multiplexing frame and comprising data corresponding to a first destination time slot (slot number of CBR slot 1) used for and the second subpakcet being associated with a second source time slot (slot number of slot 2) in the time division multiplexing frame and comprising the data corresponding to a second destination time slot (slot number of CBR slot 2, FIG. 5);

(c) a logic circuit (44 of FIG. 2 and 3) for generating a packet (70 of FIG. 5) including the first subpacket including the first subpacket and the second subpacket, the packet comprising data corresponding to a synchronization tag identifying the synchronization interval (slot number of CBR slot in FIG. 5) in which the first subpacket and the second subpacket were formatted (frame 70 in FIG. 5);

(d) a logic circuit (44 of FIG. 2 and 3) for asynchronously transmitting the packet

across an asynchronous packet switch (Lines 27-30, Col. 28; or packets transmitted between Ethernet network switches such as traffic between 54 and 56, notice that the medium connecting switches is asynchronous); and

(e) a logic circuit (44 of FIG. 2 and 3) for extracting the subpackets from the packet and storing the subpackets in a first buffer (the buffer holding the subframe for CBR slot 1) and a second buffer (the buffer holding the subframe for CBR slot 2) based on the data corresponding to the first destination time slot information and data corresponding to the second destination time slot information, the first buffer being associated with the first destination time slot (data in CBR slot 1 of 70) and the second buffer being associated with the second destination time slot (data in CBR slot 2 of 70), the arrangement of subpackets within the buffers being determined by corresponding to a synchronization tag (the synchronization timing signal for CBR, FIG. 5) identifying the synchronization interval during which the subpacket was generated plus a known fixed delay offset (CBR transmission delay between two time slots is known, line 61-65, Col. 29).

Keenan is silent on that the time slot identifier is stored within the respective subpacket.

In the same field of endeavor (data communication), Luby teaches including time slot information into each packet (“The sender places into each packet the time slot index”, Line 10 of Page 8).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Keenan and Luby to use the subpacket including

the relevant time slot identifier as taught by Luby as the subpacket taught by Keenan for the benefit of providing more detailed information of the data in the subpacket for the receiver.

For **claim 3**, Keenan in view of Luby discloses a method for transferring data (data transfer associated with the system 44 of FIG. 2 and 3) for transferring data comprising:

(a) packetizing a plurality of time-sensitive synchronous serial data source (data sources from telephone 38 and 39 of FIG. 3, which are time sensitive) related to a plurality of source time slots in a time-division multiplexing frame (TDM frame 70 of FIG 5) into first subpacket and second subpacket during a first synchronous parallel data units (data for CBR Slot 1-4 in 70, FIG. 6 in view of 52 of FIG. 3), in accordance with a synchronous clock signal ("the system Master Clock", line 51 of Col. 28) (Notice that (a) is regarding conversion from circuit switched network to packet switched network, which is clearly disclosed either in FIG. 3 or in FIG. 4);

(b) asynchronously transmitting at least the first subpacket ("CBR slot 1 8 octets" in frame 70 of FIG. 5) and a second subpacket ("CBR slot 2, 8 octets" in frame 70 of FIG. 5) in accordance with the synchronous packet switch (Ethernet switch system 44, FIG. 3);

(c) reconverting the first subpacket and second subpacket, based on the data corresponding to the first destination time slot information and data corresponding to the second destination time slot information stored within the respective first subpacket and second supacket, into synchronous data streams (data frame 70 of FIG. 5, that

comprises the first [CBR slot 1] subpacket and second [CBR slot 2] subpacket) comprising a first destination time slot and a second data stream associated with a second destination time slot, and the first subpacket and the second subpacket reconverted during a second synchronization interval having a known a known fixed delay to the first synchronization interval (line 61-65, Col. 29, CBR transmission delay between two time slots is known).

Keenan is silent on that the time slot identifier is stored within the respective subpacket.

In the same field of endeavor (data communication), Luby teaches including time slot information into each packet ("The sender places into each packet the time slot index", Line 10 of Page 8).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Keenan and Luby to use the subpacket including the relevant time slot identifier as taught by Luby as the subpacket taught by Keenan for the benefit of providing more detailed information of the data in the subpacket for the receiver.

For **claim 10**, Keenan discloses a method and an apparatus (router 44 of FIG. 2 and 3) for transferring data comprising:

(a) a source of synchronization signals defining a plurality synchronization intervals (the synchronization source of router 44);

source subpacket (data sources from telephone 38 and 39 of FIG. 3, which are time sensitive) related to a plurality of

(b) an interface for packetizing a plurality of synchronous serial data streams (synchronous serial data streams from telephone 38 and 39 of FIG. 3) relating to source time slots in a time-division multiplexing frame (TDM frame 70 of FIG 5) into respective first subpacket and second subpacket during a first synchronous parallel data units (data for CBR Slot 1-4 in 70, FIG. 6 in view of 52 of FIG. 3), the first subpacket associated with a first source time slot in a time-drivision multiplexing frame and comprsing data corresponding to a first destination time slot information (slot number of CBR slot 1) used for and the second subpakcet being associated with a second source time slot (slot number of slot 2) in the time division multiplexing frame and comprising the data corresponding to a second destination time slot information (slot number of CBR slot 2, FIG. 5);

(c) a mechanism for asynchronously transmitting at least the first subpacket ("CBR slot 1 8 octets" in frame 70 of FIG. 5) and a second subpacket ("CBR slot 2 8 octets" in frame 70 of FIG. 5) in accordance with the synchronous packet switch (Ethernet switch system 44, FIG. 3);

(d) an interface for reformatting the first subpacket and second subpacket, based on the data corresponding to the first destination time slot identifier and data corresponding to the second destination time slot identifier stored within the respective subpackets, into synchronous data streams (data frame 70 of FIG. 5, that comprises the first [CBR slot 1] and second [CBR slot 2] subpackets) comprising a first destination time slot and a second data stream associated with a second destination time slot, and the first subpacket and the second subpacket reconverted during a second

synchronization interval having a known a known fixed delay to the first synchronization interval (line 61-65, Col. 29, CBR transmission delay between two time slots is known).

Keenan is silent on that the time slot identifier is stored within the respective subpacket.

In the same field of endeavor (data communication), Luby teaches including time slot information into each packet ("The sender places into each packet the time slot index", Line 10 of Page 8).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Keenan and Luby to use the subpacket including the relevant time slot identifier as taught by Luby as the subpacket taught by Keenan for the benefit of providing more detailed information of the data in the subpacket for the receiver.

As to **claim 4** and **11**, Keenan in view of Luby discloses claim 3 and 10, wherein (a) comprises:

(a1) converting the synchronous serial data streams into synchronous parallel data units (TDM unit 61 of FIG. 3 converts synchronous parallel data units of telephone synchronous parallel data units of CBR TDM data unit 52 of FIG. 3).

As to **claim 5** and **12**, Keenan in view of Luby discloses claim 4 and 11, wherein (a) comprises: (a2) formatting the synchronous parallel data units into a respective subpacket during a first synchronization interval (the synchronous parallel data units from unit 52 of FIG. 3 are formated into respective subpackets in frame 70 of FIG. 6).

As to **claim 6**, Keenan in view of Luby discloses the method of claim 5 wherein

(b) comprises:

(b1) generating a packet (frame 70 of FIG. 6) from a plurality of subpackets (the subpackets in frame 70 of FIG. 6),

the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data units (as disclosed in parent claim 5), and a destination time slot identifier associated with each subpacket (as disclosed in parent claim 3).

As to **claim 7**, Keenan in view of Luby discloses the method of claim 6 wherein (b) comprises:

(b2) asynchronously transmitting the subpackets through an asynchronous packet switch (Switch 44 of FIG. 2-3) as part of the packet (data received at Ethernet unit 54 of FIG. 3 and then transmitted to end devices 38 or 39; or Lines 27-30, Col. 28).

As to **claims 13-14**, they the corresponding apparatus claims of claim 6-7, therefore, are rejected for the same reason explained above.

As to **claim 8** and **15**, Keenan in view of Luby discloses the method of claim 3 and 10 wherein (c) comprises:

(c1) extracting the subpackets from the packet (Line 41-44, col. 28), and

(c2) storing the subpackets into a plurality of buffers (buffers holding the subpackets; or Queue 58 of FIG. 3), each of the buffers associated with a destination time slot (the time slot associated with the subpacket), the arrangement of subpackets within the buffers being determined by a value representing the first synchronization interval plus a fixed delay offset (128μs, Line 46 of Col. 28).

As to **claim 9** and **16**, Keenan in view of Luby discloses claim 8 and 15, wherein (c) comprises:

(c3) reading the subpackets from the buffers as a plurality of parallel data units (data for CBR Slot 1-4 in 70, FIG. 6, with data for each time slot be considered as a data unit); and

(c4) converting the parallel data units into synchronous serial data streams (data from 61 to 52 in FIG.3).

For **claim 17**, Keenan discloses an apparatus comprising:

(a) an asynchronous switch (switch 44 of Fig. 2 or 3, or 4);

(b) a plurality of circuit server modules coupled to the asynchronous switch, the server modules (8 User Port Ethernet Switch Card 54 with Adapter 46, Fig. 3 and 4) comprising: (i) a time division multiplex interface (Interface to TDM 58, or interface to telephone 38, Fig 3;); and (ii) data adaptation logic (data adaptation logic of 54 or 46, Fig 4; used to data from TDM 58 or Ethernet SAR 66 of Fig. 3; or data adaptation logic of adapter 46 for adapting attached devices telephone 18 and PC 10 and etc.); and

(c) a source of synchronous clock signals (“the system Master Clock”, line 51 of Col. 28) coupled to each of the circuit server modules, the synchronous clock signals defining a plurality of synchronization intervals (the system clock of switch 44 of Fig. 2 or 3, or 4; switch 44 must have a source of synchronous clock signals in order to handle TDM, which is a common knowledge in the art);

the circuit server modules configured to perform synchronous time slot switching of synchronous data in a time-drivision multiplexing frame (TDM frame 70 of FIG 5)

across the asynchronous packet switch by asynchronously transmitting packets of the synchronous data across the asynchronous packet switch (as shown in FIG. 2-4), the packets comprising at least a first subpacket being associated with a first source time slot in a time-division multiplexing frame ("CBR slot 1 8 octets" in frame 70 of FIG. 5) and comprising data corresponding to a first destination time slot information and a second subpakcet being associated with a second source time slot in the time division multiplexing frame ("CBR slot 2 8 octets" in frame 70 of FIG. 5) and comprising the data (packet Data 305 for time slot 2" in frame 70 of FIG. 5) corresponding to a second destination time slot information (slot number of CBR slot 2);

Keenan is silent on the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data units, and a destination time slot identifier associated with each subpacket.

Luby teaches including time slot information ("The sender places into each packet the time slot index", Line 10 of Page 8) and other information (Line 7 of Page 8) into each packet.

Keenan and Luby teach the same art, one skilled in the art would be motivated to combine them together for the benefit of providing more detailed information for the receiver.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine them together for the benefit of providing more information for the receiver.

As to **claim 18**, Keenan in view of Luby discloses the apparatus of claim 17,

Keenan further discloses the time division multiplex interface comprises: serial to parallel conversion logic for converting synchronous serial data streams into parallel data units (Switch 44 of Fig. 3 converts synchronous serial data streams from Ethernet 66 into parallel data to TDM 58).

As to **claim 19**, Keenan in view of Luby discloses the apparatus of claim 17, Keenan further discloses: parallel-to-serial conversion logic for converting a plurality of parallel data units into synchronous serial data streams (Switch 44 of Fig. 3 converts parallel data to TDM 58 into synchronous serial data streams from Ethernet 66).

As to **claim 20**, Keenan in view of Luby discloses the apparatus of claim 18; Keenan further discloses an ingress data memory (TDM Flow Queue , lines 14-15, Col. 28) coupled to the time division multiplexed interface (38 or 39 of FIG. 3); an ingress context memory (Timing and Control logic, line 18 of Col. 28; or 46 of FIG. 3); and subpacket construction logic (54 of FIG. 3) for constructing in the ingress data memory a plurality of subpackets during one of the synchronization intervals (72 of FIG. 7), each subpacket associated with a source time slot and containing parallel data derived from a synchronous serial data stream (data in CBR Slot, 72 of FIG. 7) received through the time division multiplexed interface subpacket.

As to **claim 21**, Keenan in view of Luby discloses the apparatus of claim 20; Keenan further discloses the context data **comprising** destination time slot information (CBR slot 1-4, FIG. 5); Luby further discloses the destination time slot identifier (*time slot index*, line 10 of Page 8) and other information (Line 7 of Page 8) into each packet, as also suggested by Ethridge (Lines 24-27 of Col 13).

As to **claim 22**, Keenan in view of discloses the apparatus of claim 21, Keenan further discloses the data adaptation layer comprises: an ingress queue (TX TDM Flow Queue, 58 of FIG. 3) coupled to the asynchronous switch (59 of FIG. 3); and packet construction logic for constructing in the ingress queue a packet including a plurality of subpackets and the respective context data associated with each subpacket (61 of FIG. 3).

As to **claim 23**, Keenan in view of Luby discloses the apparatus of claim 22, Luby further discloses wherein the packet further comprises data identifying the synchronization interval during which the subpackets contained therein were constructed (*time slot index*, line 10 of Page 8).

As to **claim 24**, Keenan in view of Luby discloses the apparatus of claim 17, Keenan further discloses an egress data memory having a plurality of playout buffers associated with a plurality of destination time slots (buffers in Adaptor 46 of FIG; or Queue 58 of FIG. 3); and depacketizing logic for receiving a packet form the asynchronous switch and for storing subpackets contained therein into the plurality of playout buffers in the egress data memory (Adapter 46 of FIG. 3)

As to **claim 25**, Keenan in view of Luby discloses the apparatus of claim 24 Keenan further discloses wherein the data adaptation layer further comprises: playout logic (Adapter 46 of FIG. 3) for synchronously supplying parallel data from the playout buffers (Queue 58 of FIG. 3 or buffers holding frame 70 of FIG. 6) to the time division multiplexed interface (TDM Interface 61 of FIG. 3).

For **claim 26**, Keenan discloses a memory for storing data to be processed by a

data processing system including an asynchronous switch, the memory comprising:

a data structure stored in the memory and usable to perform time slot switching of data (Queue 58 of FIG. 3 or buffers in Adapter 46 of FIG. 3), the data structure comprising:

a packet comprising (FIG. 8) comprising at least first subpacket (CBR slot 1, FIG. 5) associated with a first source time slot (CBR slot 1, FIG. 5) in a time-division multiplexing frame (frame 70 in FIG. 5) and comprising data corresponding to a first destination time slot (time slot of CBR slot 1) associated with a first buffer (the buffer holding for subpacket for slot 1) and a second subpacket (CBR slot 2, FIG. 5) associated with a second source time slot (slot number of CBR slot 2, FIG. 5) in a time-division multiplexing frame (frame 70, FIG. 5) and comprising data corresponding to a second destination slot, associated with a second buffer; (the buffer holding for subpacket for slot 2), the plurality of supackets containing parallel data derived from a synchronous serial data stream (data for CBR Slots in 72 of FIG. 8), each subpacket constructed during a common synchronization interval (as shown in frame 70 in FIG. 5);

data corresponding to a synchronization tag in the packet identifying the common synchronization interval during which the plurality of subpackets were constructed and determing the arrangement of the plurality of subpackets within the first buffer and the second buffer; and data identifying the number of subpackets contained within the data structure;

Keenan is silent on the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data

units, and a destination time slot identifier associated with each subpacket.

Luby teaches including time slot information ("The sender places into each packet the time slot index", Line 10 of Page 8) and other information (Line 7 of Page 8) into each packet.

Keenan and Luby teach the same art, one skilled in the art would be motivated to combine them together for the benefit of providing more detailed information for the receiver.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine them together for the benefit of providing more information for the receiver.

As to **claim 27**, it is rejected because it is a corresponding computer program product claim of claim 1.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jianye Wu whose telephone number is (571)270-1665. The examiner can normally be reached on Monday to Friday, 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571)272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jianye Wu/

Examiner, Art Unit 2416

/Kevin C. Harper/

Primary Examiner, Art Unit 2416